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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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HEWLETT PACKARD COMPANY
P O BOX 272400, 3404 E. HARMONY ROAD
INTELLECTUAL PROPERTY ADMINISTRATION
FORT COLLINS, CO 80527-2400

EXAMINER

WILSON, YOLANDA L

ART UNIT PAPER NUMBER

2113

DATE MAILED: 09/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/765,581

Applicant(s)

JOHNSON ET AL.

Examiner

Yolanda L. Wilson

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 27 January 2004.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-25 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-25 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date <u>01/27/04</u> | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-3,5,7-9,15-25 are rejected under 35 U.S.C. 102(e) as being anticipated by Bailis et al. (US Publication Number 20030110429A1). As per claim 1, Bailis et al. discloses a first device arranged on a circuit board; and a programmable capture device arranged on said circuit board, wherein at least one input pin of said programmable capture device is communicatively coupled to at least one signal pin of said first device such that said programmable capture device captures at least one signal from said first device during testing of said first device on pages 1 and 2, paragraph 0015; on page 3, paragraph 0035. The first device is the ASIC. The programmable capture device is the FPGA.
3. As per claim 2, Bailis et al. discloses wherein said first device is arranged on a first side of said circuit board, and wherein said programmable capture device is arranged on a side of said circuit board opposite said first side see Figure 3.

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4. As per claim 3, Bailis et al. discloses wherein said programmable capture device comprises pins having an arrangement corresponding to an arrangement of pins of the first device on pages 2 and 3, paragraph 0034.

5. As per claim 5, Bailis et al. discloses wherein said programmable capture device has a density of input pins on the order of signal pins of said first device on pages 2 and 3, paragraph 0034.

6. As per claim 7, Bailis et al. discloses wherein said first device comprises an Application-Specific Integrated Circuit (ASIC) on pages 1 and 2, paragraph 0015.

7. As per claim 8, Bailis et al. discloses wherein said programmable capture device comprises a Field Programmable Gate Array (FPGA) on pages 1 and 2, paragraph 0015.

8. As per claim 9, Bailis et al. discloses at least one output pin of said programmable capture device communicatively coupled to an interface for a logic analyzer that is external to said circuit board, wherein said interface is arranged on said circuit board see Figure 4 on page 3, paragraph 0035.

9. As per claim 15, Bailis et al. discloses triggering testing of a first device arranged on a circuit board; and capturing data from said first device during said testing by a field-programmable data capture device arranged on said circuit board on pages 1 and 2, paragraph 0015; on page 3, paragraph 0035.

10. As per claim 16, Bailis et al. discloses outputting at least a portion of the captured data from the field-programmable data capture device to a logic analyzer arranged external to said circuit board on page 3, paragraph 0035.

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11. As per claim 17, Bailis et al. discloses programming the field-programmable data capture device to capture desired data from the first device on page 3, paragraph 0035; on pages 1 and 2, paragraph 0015.

12. As per claim 18, Bailis et al. discloses wherein said programming comprises: programming the field-programmable data capture device while said field-programmable data capture device is arranged on said circuit board on page 3, paragraph 0035; on pages 1 and 2, paragraph 0015.

13. As per claim 19, Bailis et al. discloses communicatively coupling a control system to said field-programmable data capture device arranged on said circuit board for performing the programming on page 3, paragraphs 0035,0042.

14. As per claim 20, Bailis et al. discloses wherein the programming comprises selecting at least one signal pin of said first device from which data is to be captured by said field-programmable data capture device on page 3, paragraph 0035.

15. As per claim 21, Bailis et al. discloses a first means for performing an operation, wherein said first means is arranged on a circuit board; and a means, arranged on said circuit board, for capturing signals from said first means during testing of said first means, wherein the capturing means is programmable while arranged on said circuit board on pages 1 and 2, paragraph 0015; on page 3, paragraph 0035.

16. As per claim 22, Bailis et al. discloses a means, arranged external to said circuit board, for analyzing captured signals of the first means, wherein the analyzing means is communicatively coupled to the capturing means on page 3, paragraph 0035.

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17. As per claim 23, Bailis et al. discloses means, arranged external to said circuit board, for programming the capturing means on page 3, paragraph 0035,0042.

18. As per claim 24, Bailis et al. discloses wherein the programming comprises selecting at least one signal pin of the first means from which signals are to be captured by the capturing means on page 3, paragraph 0035,0042.

19. As per claim 25, Bailis et al. discloses wherein the capturing means comprises a plurality of input pins that are each communicatively coupled to a different signal pin of the first means, and wherein the capturing means is programmable to select at least one of said input pins that is to have its received signals output at an output pin of the capturing means on pages 1 and 2, paragraph 0015; on page 3, paragraph 0035.

Claim Rejections - 35 USC § 103

20. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

21. Claims 4,6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bailis et al. in view of Murphy (USPN 5287617A). As per claims 4,6. The system of claim 3 wherein said first device comprises at least one-thousand signal pins.

Murphy discloses this limitation in column 1, lines 9-12

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have said first device comprises at least one-thousand

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signal pins. A person of ordinary skill in the art would have been motivated to have said first device comprises at least one-thousand signal pins because an integrated circuit can have a few pins to over a thousand pins.

22. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bailis et al. in view of Josephson et al. (USPN 5530706A).

23. As per claim 10, Bailis et al. fails to explicitly state wherein said testing of said first device comprises testing said first device at its normal operating frequency.

Josephson et al. discloses this limitation in column 1, line 65 – column 2, line 2.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have said testing of said first device comprises testing said first device at its normal operating frequency. A person of ordinary skill in the art would have been motivated to have said testing of said first device comprises testing said first device at its normal operating frequency because there is no compromising of the integrity of the data being captured from the device at normal operating frequency in spite of the clocking of the test circuitry, see column 1, lines 54-58.

24. Claims 11,12,13,14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bailis et al. in view of Josephson et al. (USPN 5530706A) in further view of DenBeste et al. (USPN 4558422).

25. As per claim 11, Bailis et al. fails to explicitly state wherein said logic analyzer has an operational frequency slower than the normal operating frequency of said first device, and wherein said programmable capture device buffers captured signals from

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the first device and outputs the captured signals at a frequency supported by the logic analyzer.

DenBeste et al. discloses this limitation in column 1, lines 35-53.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have said logic analyzer have an operational frequency slower than the normal operating frequency of said first device, and wherein said programmable capture device buffers captured signals from the first device and outputs the captured signals at a frequency supported by the logic analyzer. A person of ordinary skill in the art would have been motivated to have said logic analyzer have an operational frequency slower than the normal operating frequency of said first device, and wherein said programmable capture device buffers captured signals from the first device and outputs the captured signals at a frequency supported by the logic analyzer because data can be captured at different frequencies.

26. As per claim 12, Bailis et al. discloses wherein the programmable capture device parallelizes the captured signals on page 3, paragraph 0042.

27. As per claim 13, Bailis et al fails to explicitly state wherein said logic analyzer has an operational frequency greater than the normal operating frequency of said first device, and wherein said programmable capture device buffers captured signals from the first device and outputs the captured signals at a frequency supported by the logic analyzer.

DenBeste et al. discloses this limitation in column 1, lines 35-53.

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Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have said logic analyzer have an operational frequency greater than the normal operating frequency of said first device, and wherein said programmable capture device buffers captured signals from the first device and outputs the captured signals at a frequency supported by the logic analyzer. A person of ordinary skill in the art would have been motivated to have said logic analyzer have an operational frequency greater than the normal operating frequency of said first device, and wherein said programmable capture device buffers captured signals from the first device and outputs the captured signals at a frequency supported by the logic analyzer because data can be captured at different frequencies.

28. As per claim 14, Bailis et al. discloses wherein the programmable capture device serializes the captured signals on page 3, paragraph 0042.

Specification

29. The abstract of the disclosure is objected to because it is not describing the invention. It is written like a claim would be. Correction is required. See MPEP § 608.01(b).


Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yolanda L. Wilson whose telephone number is (571) 272-3653. The examiner can normally be reached on M-F (7:30-4:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571) 272-3645. The fax phone

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number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.


Yolanda L. Wilson
Examiner
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